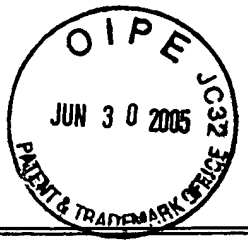
AFV ZPW

S/N 10/084,543



PATENT
Atty. Docket No. FR920010006US1

CERTIFICATE OF MAILING (37 C.F.R. 1.8(a))
I hereby certify this correspondence is being deposited with the United States Postal service with sufficient postage as first class mail in an envelope addressed to: Mail Stop Appeal Brief-Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450
on June 27, 2005
by KAREN ORZECHOWSKI **Signature:** Karen Orzechowski

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of R. Gallezot et al	:	Date: June 27, 2005 IBM Corporation - IP Law YXSA/B002 P.O. Box 12195
Serial No. 10/084,543	:	Research Triangle Park, North Carolina 27709
Filed: 27 February 2002	:	
For: System and Methods for Enabling Computation of CRCs N-bit at a Time	:	Unit: 2133
	:	Examiner: J.D. Torres

Mail Stop Appeal Brief- Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF
(PATENT APPLICATION-37 CFR 1.192)

Sir:

1. Transmitted herewith in triplicate is the APPEAL BRIEF in this application with respect to the Notice of Appeal filed on June 3, 2005.

2. STATUS OF APPLICANT

This application is on behalf of

_X_ other than a small entity
___ small entity
verified statement: ___ attached ___ already filed

3. **FEE FOR FILING APPEAL BRIEF**

Pursuant to 37 CFR 1.17(f) the fee for filing the Appeal Brief is:

___ Small entity $250.00
_X_ Other than a small entity $500.00

Appeal Brief fee due: $ 500.00_____

4. **EXTENSION OF TERM**

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136 apply.

___ (a) Application petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d)) for the total number of months checked below:

Extension (months)	Fee for other than a small entity
___ one month	$ 110.00
___ two months	$ 450.00
___ three months	$1,020.00
___ four months	$1,590.00

____ (b) Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

5. **TOTAL FEE DUE**

The total fee due is:

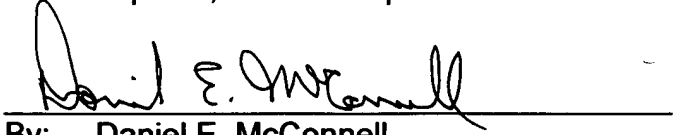
Appeal brief fee _____ $ 500.00__
Extension fee (if any) _ $ .00_____
TOTAL FEE DUE ___$500.00__

6. **FEE PAYMENT**

___ Attached is a check in the sum of $ _____
_X_ Charge Account No. **50-0563** the sum of **$500.00**
(a duplicate of this transmittal is attached)

7. **FEE DEFICIENCY**

_X If any additional extension and/or fee is required, this is a request therefor and to charge Account No. 50-0563.



By: Daniel E. McConnell,
Attorney of Record Reg. No.: 20,360

Tel: 919- 510 4246 Fax: 919-254-2649

Certificate of Mailing/Facsimile 37 CFR 1.8(a)

I hereby certify that this correspondence is being:

X deposited with the United States Postal Service as first class mail in an envelope with sufficient postage addressed to:

COMMISSIONER OF PATENTS
P.O. Box 1450
Alexandria, VA 22313-1450

_____ transmitted by facsimile to 703 872 9306

on June 27, 2005

By KAREN ORZECHOWSKI Karen Orzechowski

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	:	Date: June 27, 2005
R. Gallezot et al	:	Group Art Unit: 2133
Serial Number: 10/084,543	:	Examiner: J.D. Torres
Filed: 27 February 2002	:	INTERNATIONAL BUSINESS MACHINES CORPORATION
Title: System and Methods for Enabling Computation of CRC's N – bit at a Time	:	Intellectual Property Law Department D-YXSA B-002/2 P.O. Box 12195
07/01/2005 SSITHIB1 00000040 500563 10084543	:	Research Triangle Park, NC 27709
01 FC:1402 500.00 DA		

Brief on Appeal

The Commissioner of Patents
P.O. Box 1450
Alexandria, VA 2213-1450

Dear Sir:

Applicants have given Notice of Appeal from a Final Rejection in this application.

Real Party in Interest

The real party in interest in this appeal is the assignee, International Business Machines Corporation.

Related appeals and interferences

There are no related appeals or interferences.

Status of claims

Claims 1 through 9, 12, 13 and 15 through 20 are presented.

Claim 4 is objected to.

Claim 20 is deemed withdrawn from consideration.

Claims 1 through 3, 5 through 9, 12, 13 and 15 through 19 are under Final Rejection.

Claims 1 through 3, 5 through 9, 12, 13 and 16 through 19 are under Final Rejection under 35 USC 102 as being anticipated by the teachings of Freeman U.S. Pat. 3,678,469.

Claim 15 is under Final Rejection under 35 USC 103 as being obvious from the teachings of Freeman U.S. Pat. 3,678,469.

Claims 4 and 19 are rejected under 35 USC 112 as indefinite. No explanation is given of the supposed shortcoming of Claim 19. Claim 4 is found indefinite because of a supposed lack of an antecedent for a limitation to an "N-bit

chuck".

Summary of claimed subject matter

Claim 13, addressed below, is the only claim presented which includes a limitation set forth in "means and function" language so as to require specific reference to the specification and drawings.

The Examiner has objected to all claims on the ground that reference characters are included in the claims. This objection is believed contrary to MPEP 608.01(m), third paragraph, as will be pointed out below in the Argument portion of this Brief.

The present invention relates to the calculation of Cyclic Redundancy Check (CRC) codes and more particularly to a general method for computing such codes N-bits at a time. As acknowledged (and evidenced by the age of the Examiner's sole prior art reference, which issued in 1972), Cyclic Redundancy Checking (CRC) has long been, and still remains, the technique of choice for verifying the integrity of messages transmitted over communications networks. As the name suggests, redundant information, under the form of a digest computed on the entire message, is appended at the end of each transmitted message so as the recipient is made capable of verifying that the message has not been corrupted en route.

Most communications protocols and standards, if not all, make use of CRC's. To specify the way a particular CRC should be used, protocols or standards always explain and describe their CRC through a particular model based on a Linear Feedback Shift Register or LFSR. While this approach is simple (one may just ignore the mathematics on which CRC is actually based, which is generally considered as an advantage) it tends, however, to favor a bit-wise or one bit at a time computation of CRC's similar to LFSR structure. This kind of implementation

used to be an acceptable solution to the actual implementation of CRC's but the dramatic increase in the speed of the communications lines, now commonly measured in gigabits or tenth of gigabits per second, renders the one-bit-at-a-time type of processing totally inadequate. This is the problem addressed by this invention.

In this application, a method and apparatus are disclosed for performing a Cyclic Redundancy Check (CRC) calculation, N-bits at a time, over a binary string of data bits. The CRC calculation is based on a generator polynomial G(X) of degree d. It has intermediate and final results fitting a d-bit wide Field Check Sequence (FCS). The generator polynomial allows forming a multiplicative cyclic group comprised of d-bit wide binary vectors. The iterative calculation method teaches that, at each loop, a new N-bit chunk of data bits is picked from the binary string of data bits (See Claims 1, 16 and 20; specification page 17, beginning at line 1; Fig. 11). It is divided, modulo the generator polynomial G(X), to obtain a d-bit wide division result (See Claims 1, 16 and 20; specification page 17, beginning at line 1; Fig. 11). Meanwhile, a current value of the d-bit wide FCS, considered as one of the d-bit wide binary vectors, is displaced in the multiplicative cyclic group, of a value corresponding to N. Then, the d-bit wide division result and the displaced d-bit wide Field Check Sequence or FCS are added modulo two and used to update the FCS. The above steps are re-executed until no data are left of the binary string of data bits thus, getting the final result of the CRC calculation which can be used either for checking a message already including a FCS or for the generation of this FCS. The method of the invention allows a forward (from MSB) or backward (from LSB) calculation of CRC's.

Claim 2 is patentably distinct from Claim 1, from which it depends, by the recitation that the final result of the CRC calculation is used to generate the d-bit wide FCS (specification page 11, beginning at line 23; Fig. 5).

Claim 3 is a multiple dependency claim, depending from one of Claim 1 or Claim 2 and is patentably distinct from each of those antecedent claims by the recitation that the final CRC result is a checking result of the binary string including the FCS (specification page 11, beginning at line 23; Fig. 5).

Claim 4 depends from Claim 1 and is patentably distinct from that claim by the recitation that the dividing step of the base claim is omitted under defined circumstances(specification page 11, beginning at line 23; Fig. 5). Claim 4 was rejected under 35 USC 112 for a supposed recitation of "N-bit chucks". However, there is no such recitation in the amended claim here under consideration and the rejection is thus not understood by applicants' undersigned attorney.

Claim 5 depends from Claim 4 and is patentably distinct from that claim by the recitation that the data is padded if the value of the N-bit chunk is below a defined value (specification page 12, line 8).

Claim 6 depends from Claim 1 and is patentably distinct from that claim by the recitation that the CRC calculation is done from the most significant bit and with forward multiplication (specification page 11, line 32 et seq.)

Claim 7 depends from Claim 1 and is patentably distinct from that claim by a recitation which is an inverse of the recitations of Claim 6. That is, the CRC calculation is done from the least significant bit and backward multiplication is used (specification page 15, line 1 et seq; Fig. 7).

Claim 8 depends from Claim 1 and is patentably distinct from that claim by the recitation of the environment – a frame or message moved over a communications network – in which the invention is implemented (specification page 6, beginning at line 3).

Claim 9 depends from Claim 1 and is patentably distinct form that claim by the recitation of another environment in which the invention is implemented, the derivation or storage of a file in a computer system (specification page 7, beginning at line 22).

Claims 10 and 11 have been canceled and are not here under consideration.

Claim 12 is an apparatus claim multiply dependent upon the methods recited in Claims 1 or 2. The claim recites a processor which executes instructions carrying out CRC calculations according to those methods (specification page 18, beginning at line 20; Fig. 14).

Claim 13 is the sole claim under consideration which includes a recitation in "means and function" language, with a recitation of a state machine comprising means adapted for carrying out the method according to Claim 1 or Claim 2. Claim 13 is an apparatus claim multiply dependent upon the methods recited in Claims 1 or 2. The state machine is described in the specification on page 16, beginning at line 10, where reference is made to Figures 5, 6 and 10.

Claim 14 has been canceled and is not here under consideration.

Claim 15 is an apparatus claim to a computer readable medium comprising instruction for carrying out the methods according to one of Claim 1 or Claim 2 (specification page 18, beginning at line 20; Fig. 14). This is the only claim rejected under 35 USC 103 for obviousness.

Claim 16 is a independent method claim patentably distinguished from Claim 1 by focusing on the process steps which generate and update an FCS. The enabling disclosure in the specification is found as indicated above in the introductory general discussion, pages 3 and 4 of this Brief.

Claim 17 depends from Claim 16 and differs patentably therefrom by recitations of the steps which check for necessity of looping through the acts of the independent claim and then doing so under defined circumstances.

Claim 19 depends from Claim 1 and is the claim which contains a misspelling of "chunk" as "chuck", leading to the 35 USC 112 rejection erroneously made of Claim 4. Upon allowance after appeal this claim will be amended to correct this plain typographical error.

Claim 20 is a program product claim and has been held to be withdrawn from consideration in this proceeding. This is believed error and it is submitted that the claim should be considered with the remaining claims in the application. Claim 15, which is under consideration here, is also a program product claim. The difference between the two, which gives rise to separate patentability, is that Claim 15 is multiply dependent upon method claims while Claim 20 sets out instruction modules which, when executing, generate the method steps.

Grounds of rejection to be reviewed

Claim 1 stands Finally Rejected under 35 USC 102(b) as anticipated by the teachings of Freeman U.S. Pat 3,678,469.

Claim 2 stands Finally Rejected under 35 USC 102(b) as anticipated by the teachings of Freeman U.S. Pat 3,678,469. However, the rejection makes reference to a Fig. 1 of Cassidy, a reference not otherwise identified and thus not clearly known to applicants' undersigned attorney. This reference suggests that the rejection is for obviousness under 35 USC 103, but it is less than clear from the record.

Claim 3 stands Finally Rejected under 35 USC 102(b) as anticipated by the

teachings of Freeman U.S. Pat 3,678,469.

Claim 4 is not rejected on art and erroneously rejected under 35 USC 112 as indefinite.

Claim 5 stands Finally Rejected under 35 USC 102(b) as anticipated by the teachings of Freeman U.S. Pat 3,678,469.

Claim 6 stands Finally Rejected under 35 USC 102(b) as anticipated by the teachings of Freeman U.S. Pat 3,678,469.

Claim 7 stands Finally Rejected under 35 USC 102(b) as anticipated by the teachings of Freeman U.S. Pat 3,678,469.

Claim 8 stands Finally Rejected under 35 USC 102(b) as anticipated by the teachings of Freeman U.S. Pat 3,678,469.

Claim 9 stands Finally Rejected under 35 USC 102(b) as anticipated by the teachings of Freeman U.S. Pat 3,678,469.

Claim 12 stands Finally Rejected under 35 USC 102(b) as anticipated by the teachings of Freeman U.S. Pat 3,678,469.

Claim 13 stands Finally Rejected under 35 USC 102(b) as anticipated by the teachings of Freeman U.S. Pat 3,678,469.

Claim 15 stands Finally Rejected under 35 USC 103 as obvious from the teachings of Freeman U.S. Pat 3,678,469 modified in view of the Examiner's bare assertion that computer software offers a flexible scalable means for implementing an error correction algorithm.

Claim 16 stands Finally Rejected under 35 USC 102(b) as anticipated by the teachings of Freeman U.S. Pat 3,678,469.

Claim 17 stands Finally Rejected under 35 USC 102(b) as anticipated by the teachings of Freeman U.S. Pat 3,678,469.

Claim 18 stands Finally Rejected under 35 USC 102(b) as anticipated by the teachings of Freeman U.S. Pat 3,678,469.

Claim 19 stands Finally Rejected under 35 USC 102(b) as anticipated by the teachings of Freeman U.S. Pat 3,678,469.

Claim 20 has been deemed by the Examiner to be withdrawn from consideration here as directed to an invention that is independent or distinct from the invention first claimed. The reason given is a possible search in a particular class and subclass. As has been pointed out, a claim of similar direction – to a program product – has previously been present in Claim 15. Accordingly, the Examiner's position is challenged. Should the Examiner adhere to this position, then it is requested that this appeal go forward with Claim 20 excluded from the appeal decision and retained solely for purpose of permitting applicants' to submit such a claim in a separate filing after decision on appeal should they so choose.

Argument

This argument will deal, in order, with the general objection to the claims on page 3 of the Official Action; the rejection under 35 USC 112 on page 5 of the Official Action; and the rejections on art beginning on page 5 of the Official Action.

As to the general objection to the claims on the ground that reference numbers are present in the claims, this is precisely what is allowed under the third

paragraph of MPEP Sect 608.01(m) where it is stated:

> "Reference characters corresponding to elements recited in the detailed description and the drawings ma be used in conjunction with the recitation of the same element or group of elements in the claims. ... The use of reference characters is to be considered as having no effect on the scope of the claims."

It would appear to applicants' undersigned attorney that the objection is groundless and that consideration of the claims should go forward as the claim format meets the stated requirements of the Office.

There is a standing objection to Claim 17 arising from the use of the word "act" in the recitation of subparagraph (g) identifying a previously recited step (d) of Claim 16. This is believed ill founded and contested here. Step (or act) (d) in Claim 16 is "updating said d-bit wide FCS". It is submitted that this recited step does produce a result – the updated FCS. The further recitation in step (g) of Claim 17 is one fork of an alternate following a determination ("checking"), the recited action being to leave the result in step (d) as the calculated CRC. The meaning appears sufficiently clear and unambiguous as to permit both examination and comprehension by others after issuance.

Turning to the rejection under 35 USC 112 for indefiniteness, it is believed that the Examiner made a typographical error in referencing Claim 4, as the questioned word is absent from that claim. The questioned word is found in the second line of Claim 19, for which the rejection lacks any detail. The offensive word is "chuck", varying by one letter from the term used throughout the other claims, "chunk". While this is an admitted inaccuracy, it is respectfully submitted that the spelling may be corrected in due course after allowance of the claims on this appeal and that, accordingly, the claim should be further considered at this time.

Turning to the first substantive rejection based on prior art, the rejection of Claim 1 under 35 USC 102(b) as anticipated by Freeman, it is axiomatic that any rejection based upon anticipation must find all elements of a rejected claim within the four corners of the reference applied. It is respectfully submitted that such a basis is lacking here, and that the rejection accordingly cannot stand.

At the outset, the implementation of Freeman fails to solve the problem to which the present invention is addressed, namely supporting CRC computation at gigabit line speeds. The general flow charts of the present invention (Fig.s 7 and 9) show two steps: dividing and multiplying. As indicated in Fig. 10, the multiplier and divider can be implemented in a single logic, enabling the computation to be done in a single clock cycle. Freeman is incapable of doing this.

The Freeman technology is disclosed in different method steps which are not at all equivalent to the claimed process. Freeman may propose processing N-bits at a time as it processes one character at a time and one character may be more than one bit. However, the array calculator performs as do the feedback type cyclic redundancy check remainder generating devices of the prior art acknowledged in the opening pages of the present specification. Freeman repeats the same prior art CRC computation calculator with dependent cells, each cell having output propagated to the next following cell and so forth. This creates a propagation delay which precludes the high speeds necessary to solve the problem addressed by the present subject invention. Freeman discloses that in Col. 3 beginning at line 8, where it is disclosed: "The output of the array calculator, after a sufficient amount of time to account for the propagation delays within the array calculator, comprises the new CRC and is stored in the new CRC register 30."

It is respectfully submitted that the steps of dividing, generating and adding recited in Claim 1 are absent from Freeman. In the present invention, these steps are performed in one entry of the entire N-bit chunk at a time (Fig. 11). With the

Freeman technology, the CRC computation is performed by entering the generator polynomial, the N-bit chunk, the old CRC and a code selection into a rectangular array calculator. Inside the calculator, the signal propagates through as many steps as the number of cells. Because the output of one cell is used as the input for the next, the propagation delay described above (in the words of Freeman) arises. Freeman teaches (Col. 1, lines 68 and 70) that the array calculator performs the same functions as the feedback type CRC remainder generating devices of the prior art, precisely the effect the invention of this application avoids. There is no disclosure or teaching in Freeman of an FCS.

It is respectfully submitted that the Freeman technology is incapable of implementing the dividing and multiplying steps in a single logic and in a single clock cycle, as is done with the technology claimed here.

With more particular reference, the first two recitations of Claim 1, picking a chunk of data and dividing the chunk, are compared by the Examiner to the cell split linear feedback register of the array calculator of Freeman. This comparison is inaccurate and false, as Freeman performs a shift by combining the generator polynomial bits, the N-bit chunk, and the old CRC bits in each cell and does not perform a separate division of the N-bit chunk alone.

Claim 1 recites generating a value for the FCS which is displaced. The Examiner asserts this element is found in the Rectangular Array Calculator of Fig. 1 of Freeman, stating that the Old CRC is displaced to generate the New CRC. Again, the Freeman array calculator combines the polynomial bits, the N-bit chunk and the old CRC bits in each cell. There is no separated function of generating a value for FCS as recited in the claim. Again, there is no disclosure or teaching in Freeman of an FCS.

In the claimed invention, the step of adding is performed between the old and

the code bits and the cell outputs but there is no adding between old and new FCS computation (Fig.s 2, 2a and 2b of Freeman).

Concluding with regard to Claim 1, the distinction between the separate steps recited in the limitations of Claim 1, and the portions of data on which those steps are performed, demonstrate the patentable distinctions of applicants' invention from the prior art applied. The recited steps as applied to the data portions recited simply are not taught by, and are impossible in, the Freeman technology.

The rejection of Claim 2 is not clearly understood. The rejection refers to Freeman teaching that the final result is stored to memory 14 in Figure 1 of Cassidy. This would suggest a 35 USC 103 obviousness rejection, but the rejection is stated to be under 35 USC 102. Freeman does disclose a memory 14 in Fig. 1. Assuming for the purposes of argument that the Examiner intended a reference to that memory, the rejection still misses the point. The teaching in no way discloses the generation of a d-bit wide FCS, which is the recited step of Claim 2. The rejection is simply inapposite and ignores the fundamental difference between Freeman and Claim 1 from which Claim 2 depends. The reference to memory fails to supply the deficiencies of Freeman as argued above.

The rejection of Claim 3 is a one sentence shorthand assertion that the new CRC in Freeman teaches that the final result is a checking result of the binary string of data including the d-bit wide FCS. No specific reference to where a teaching can be found in Freeman is given. The Examiner appears to have confused the CRC with the CRC register (see Col. 3, line 12). Unfortunately, Freeman uses the reference character 30 twice in the description, referring to two distinct elements. In Fig. 1, reference character 30 refers to the block entitled "new CRC" (see also Col. 3, lines 8 through 11, where the element is identified as a register). In Fig. 2a, the reference character 30 refers to the polynomial register (Col. 4, line 22). This difference is unreconciled. Further, applicants' undersigned attorney cannot find in

Freeman any discussion of an FCS, an element of the recitations in Claim 3. The absence of such a teaching invalidates Freeman as a reference for the claim at issue.

There is no stated rejection of Claim 4 on art. There is confusion within the Official Action as to the basis of any rejection of Claim 4, leaving applicants' undersigned attorney with no clear basis for argument against a rejection. Should the Examiner attempt to shift ground in the forthcoming Examiner's Answer, assuming for purposes of argument that immediate allowance of the application will be denied even though appropriate, then further argument may be provided.

Claim 5 is rejected with a one sentence shorthand statement referring to New Character 34 in Fig. 2a of Freeman. Again, the referenced element in Fig. 2a of Freeman is a register, which is not anticipatory of the "if ... then" recitations of Claim 5. Disclosure of a register is not the same as recitation of the step of padding. Assuming for purposes of argument that the Examiner's reference should have been to the description appearing in Col. 3 of Freeman at lines 61 through 64, the register filling described is other than the recited steps of distinguishing a level as compared with a predetermined width and then filling the N-bit chunk. Instead, the fill is of any one (or more if necessitated) of three distinct elements – the polynomial, the old CRC and the new character.

The Examiner has lumped together the rejections of Claims 6 and 7.

The claims are in fact distinct, one (Claim 6) limiting the method to starting from a most significant bit and doing a forward multiplication and the other (Claim 7) starting from a least significant bit and doing a backward multiplication.

The rejection refers to a Fig. 6 on page 166 of Freeman. The Freeman patent spans 10 columns of text (5 pages) and has figures numbered up to Fig. 5b.

The rejection refers to a Fig. 6 on page 166 of Freeman. The Freeman patent spans 10 columns of text (5 pages) and has figures numbered up to Fig. 5b. Thus the rejection stated is nonsensical. Absent any sensible position taken by the Examiner, applicants' undersigned attorney is at a loss to make a responsive argument beyond the distinctions pointed out. It is the applicants' position that there is no viable rejection of record for Claims 6 and 7 and that the claims should be immediately allowed.

The rejection of Claims 8 and 9 is similarly lumped. The Examiner's position is that the claims are directed to an intended use and that the Freeman teaching is inherently capable of being used in a networking environment or a computing system. In an anticipation rejection, inherency must necessarily follow from the teachings of the prior art. See *The Toro Co. v. Deere & Co.* 355 F.3d 1313 (Fed. Cir. 2004). A high probability of inherency is insufficient. See *Glaxo v. Novopharm Ltd.* 52 F.3d 1043 (Fed. Cir. 1995). The Examiner here has failed to suggest or support that this test is met. Instead, a simple flat statement – unsupported by fact -- has been made. It is submitted that this is plain error and that the rejection cannot stand on this basis.

Claim 12 is rejected with a simple statement that Fig. 2 in Freeman is a processor executing instructions to calculate a CRC. Freeman describes Fig. 2 as a detailed drawing of the array calculating means shown in Fig. 1. In Col. 3, beginning a line 43 and continuing through Col. 5, line 39, Freeman describes the calculating means with more specificity. The array is composed of a plurality of interconnected gates (see Fig. 3). In distinction from this arrangement, applicants' processor is disclosed in Fig. 14 and the associated text beginning on page 18 at line 20. It is submitted to be clear from applicants' disclosure that the processor recited is a stored program general purpose processor. The array calculator of Freeman is not such a processor and does not teach or suggest the storage of CRC instructions in memory for implementation by access to and execution of those

The rejection of Claim 13, while stated to be under 35 USC 102(b), makes no reference to the Freeman disclosure. The rejection is a simple bare statement asserting that a CRC calculation is a state machine function. The rejection fails the necessary test of an anticipation rejection.

Claim 15 is rejected as obviated under 35 USC 103 by Freeman. The Graham v Deere test for obviousness under 35 USC 103 is the subject matter of Section 2141 et seq in the Manual of Patent Examining Procedure. To briefly restate, the three inquiries set forth by the Court, in order, are to determine the applicable prior art, then determine the differences between that art and the claimed invention, and then determine whether a person of ordinary skill in the applicable art would know to make the modification necessary to arrive at those differences in view of the prior art applied.

As has been stated by the Court of Appeals for the Federal Circuit in considering matters on appeal from the Board of Appeals within the Patent Office, obviousness is a question of law (the Court citing Graham v Deere), but this determination occurs in the context of a factual inquiry regarding the scope and content of the prior art. This factual inquiry examines what a reference would have taught or suggested to one of ordinary skill in the art at the time the of the invention (the Court citing Northern Telecom v Datapoint Corp., 908 F.2d 931, 15 USPQ2d 1321). The Court has cautioned against focusing on the obviousness of the differences between the claimed invention and the prior art rather than the obviousness of the claimed invention as a whole as 35 USC 103 requires (citing Hybritech, Inc. v Monoclonal Antibodies, Inc., 802 F.2d 1367, 231 USPQ 81) and against the use of hindsight reconstruction of what is disclosed in a prior art reference (citing Grain Processing Corp. v American Maize Products Co., 840 F.2d 902, 5 USPQ2d 1788). The Court has quoted approvingly from its decision in In re Fritch, 972 F.2d 1260, 23 USPQ2d 1780, in which it said:

The mere fact that the prior art may [emphasis added] be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification.

On the latter point, the CAFC has said that the Patent Office, in determining the obviousness of a claimed invention that combines known elements, must determine whether there is something in the prior art as a whole to suggest the desirability, and thus the obviousness, of making the combination (citing Lindemann Maschinenfabrik GmbH v American Hoist and Derrick Co., 730 F.2d 1452, 221 USPQ 481).

It is the burden of the Examiner to establish why one having ordinary skill in the art would have been led to the claimed invention by the reasonable teachings or suggestions found in the prior art, or by a reasonable inference to the artisan contained in such teachings or suggestions. See In re Sernacker, 702 F.2d 989, 995; 217 USPQ 1, 6 (Fed. Cir. 1983). The reviewing court for the Patent Office requires proof by evidence in order to establish a *prima facie* case when the proposition at issue is not supported by a teaching in a prior art reference, common knowledge or capable of unquestionable demonstration. See In re Knapp-Monarch Co., 296 F.2d 230, 232; 132 USPQ 6, 8 (CCPA 1961) and In re Cofer , 354 F.2d 664, 668; 148 USPQ 268, 271-272 (CCPA 1966). See also Section 2143 et seq of the MPEP.

An obviousness rejection based on a single prior art reference is a special case, in which the Examiner must clearly support the assertions made. Here, there is s simple, bare, unsupported statement of what would purportedly have been known to one of ordinary skill in the art. This is plainly improper. The necessary test for an obviousness rejection has not been met.

Claim 16 was lumped with Claim 1 for a rejection under 35 USC 102(b) on

for an obviousness rejection has not been met.

Claim 16 was lumped with Claim 1 for a rejection under 35 USC 102(b) on Freeman. Claim 16 differs from Claim 1 in reciting the data manipulations around the FCS portion of data being handled. Freeman lacks any disclosure of an FCS or any such data manipulations. For this reason, the rejection fails the fundamental test of an anticipation rejection – that the anticipating teaching must be found within the four corners of the single prior art reference relied upon.

Claim 17 further characterizes the process of Claim 16 and has been rejected without an attempt to make a detailed application of the Freeman teaching to the language of the claim. Again, the rejection fails the fundamental test of an anticipation rejection – that the anticipating teaching must be found within the four corners of the single prior art reference relied upon.

Claim 18, similarly to Claim 17, further characterizes the processes of Claims 16 and 17 and has been rejected without an attempt to make a detailed application of the Freeman teaching to the language of the claim. Again, the rejection fails the fundamental test of an anticipation rejection – that the anticipating teaching must be found within the four corners of the single prior art reference relied upon.

Claim 19 further characterizes the process of Claim 1 by specifying a particular manipulation of FCS data. Freeman lacks any disclosure of an FCS or any such data manipulations. For this reason, the rejection fails the fundamental test of an anticipation rejection – that the anticipating teaching must be found within the four corners of the single prior art reference relied upon.

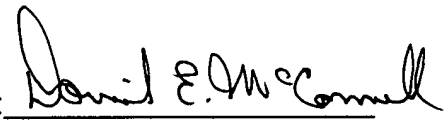
Claim 20 has been deemed by the Examiner to have been withdrawn from consideration by a constructive election (see page 2 of the detailed action of Final Rejection). It is submitted that this is error and the claim should be considered on

this appeal. In particular, Claim 20 is a program product claim. Previously considered Claim 15, on which action has been taken, is a program product claim which has been in the application from filing. Thus the Examiner has already considered such a claim, and has apparently done the necessary search to have supported a position.

Further, Claim 20 patentably distinguishes applicants' invention from the Freeman reference for many of the reasons stated above. The recitations include instruction modules which generate a value for FCS and then manipulate data to update the FCS. As pointed out above, Freeman lacks any disclosure of an FCS or any such data manipulations. For this reason, any rejection grounded on Freeman fails the fundamental test of an anticipation rejection – that the anticipating teaching must be found within the four corners of the single prior art reference relied upon.

It is respectfully submitted that, for the reasons given, each of the claims now presented in this application is allowable, and such a decision is solicited. This Brief is submitted in the requisite number of copies, and the Office is authorized to make any necessary charges against Deposit account 50-0563.

Respectfully submitted,

By: 

Daniel E. McConnell
Registration No. 20,360
(919) 510-4246

Claims appendix

1. A method of performing a Cyclic Redundancy Check (CRC) calculation, said CRC calculation done with N-bit at a time [500] over a binary string of data bits [520], said CRC calculation based on a generator polynomial G(X) [130] of degree d [131], said CRC calculation having intermediate and final results fitting a d-bit wide Field Check Sequence (FCS) [120], said generator polynomial allowing to form a multiplicative cyclic group comprised of d-bit wide binary vectors [400], said method comprising the steps of:

picking [1100] a new N-bit chunk of data bits from said binary string of data bits;

dividing [1110], modulo said generator polynomial G(X), said new N-bit chunk of data bits thus, getting a d-bit wide division result [535];

generating a value for FCS displaced within said cyclic group of d-bit wide binary vectors;

adding [1130], modulo two, said d-bit wide division result and said displaced d-bit wide FCS so generated;

updating [1140] said d-bit wide FCS;

checking if more data bits of said binary string of data bits are left for calculation:

if yes [1151], repeating all recited steps;

if not [1152], exiting the method after checking step;

thereby, getting a final result of said CRC calculation in said d-bit wide FCS.

2. The method according to claim 1 wherein said final result is utilized to generate said d-bit wide FCS [510] for said binary string of data bits.

3. The method according to claims 1 or 2 wherein said final result is a checking result of said binary string of data bits [520] including said d-bit wide FCS [510].

4. The method according to claim 1 wherein said dividing step is omitted, if value of said N-bit is equal to said degree d.

5. The method according to claim 4 wherein, if value of said N-bit is lower than said degree d, the further step of: padding said N-bit chunk of data with enough leading zeros to match said d-bit wide FCS [540].

6. The method according to claim 1 wherein said CRC calculation is done from a most significant bit (MSB) [530] of said binary string of data bits and wherein said generating step includes a forward multiplication [560] of said d-bit wide FCS.

7. The method according to claim 1 wherein said CRC calculation is done from a least significant bit (LSB) [710] of said binary string of data bits and wherein said generating step includes a backward multiplication [760] of said d-bit wide FCS.

8. The method according to claim 1 wherein said binary string of data bits is a frame or message moved over a communications network.

9. The method according to claim 1 wherein said binary string of data bits is derived or stored as a file in a computing system.

10. (Canceled)

11. (Canceled)

12. A system, in particular a processor [1400], executing instructions for carrying out CRC calculations according to the method of claims 1 or 2.

13. A system, in particular a state machine [1000] aimed at performing CRC calculations N-bit at a time, comprising means adapted for carrying out the method

according to claims 1 or 2.

14. (Canceled)

15. A computer-like readable medium comprising instructions for carrying out the methods according to claims 1 or 2.

16. A method for calculating Cyclic Redundancy Check (CRC) including the acts of:

(a) selecting N-bits, N greater than 0, of data from a binary string of data bits;

(b) generating a value for FCS displaced within said cyclic group of d-bit wide binary vectors;

(c) adding (1130) modulo two, the N-bits and said value so generated; and

(d) updating said d-bit wide FCS.

17. The method of claim 16 further including the acts of:

(e) checking if more bits of said binary string are left for calculation;

(f) if yes, repeating acts (a) through (e);

(g) if not, existing with result in act (d) being the calculated CRC.

18. The method of claims 16 or 17 further including the step of prior to performing step (b) dividing the N-bits, modulo generator polynomial G(x), to obtain a d-bit wide division result.

19. The method of claim 1 wherein generating the value includes multiplying current FCS value by a displacement corresponding to the N-bit chuck of data bits.

20. A program product including:

a media in which computer program is recorded, said computer program including first instruction module for selecting N-bits, N greater than 0, of

data from a binary string of data bits;

second instruction module generating a value for FCS displaced within said cyclic group of d-bit wide binary vectors;

third instruction module for adding module two, the N-bits and said value so generated; and

fourth instruction module, using results from third instruction module, to update said

d-bit wide FCS.

Evidence appendix

There is no evidence to be presented in this appendix.

Related proceedings appendix

There are no related proceedings materials to be presented in this appendix.